

and 23-37 are currently elected, of which claims 1, 7, 11 and 23-25 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 4 of the Official Action rejects claims 1, 6, 7, 10, 11, 14 and 23-31 as obvious based on the combination of U.S. Patent No. 6,774,877 to Nishitoba and U.S. Publication No. 2002/0047825 to Yamazaki. The Applicant respectfully traverses the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Independent claims 1, 7, 11 and 23-25 recite a same semiconductor island. For the reasons provided below, Nishitoba and Yamazaki, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

The Official Action concedes that "Nishitoba et al. fail to disclose the limitation that 'wherein the first transistor and the second transistor share a same semiconductor island', i.e. the first and second transistors are formed on the same semiconductor layer/island" (emphasis in original), but asserts that Yamazaki '825 teaches a silicon oxide film (102) and that the silicon oxide film "refers to instant claimed semiconductor island" (Paper No. 20090506, pages 5-6). The Applicant respectfully disagrees and traverses the assertions in the Official Action. A silicon oxide film is not a semiconductor island. Yamazaki '825 merely discloses "a silicon oxide film 102 as an underlayer film 102" (¶ [0044]).

In the "Response to Arguments" section, the Official Action asserts that "applicant's arguments are conclusionary [sic]," that "applicant has not explained how the silicon oxide film of Yamazaki is *not* a "semiconductor island", and applicant did not explain what the improvement is over the prior art of record" (page 7, Paper No. 20091105; emphasis in original). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

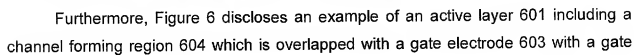
As is readily understood to those of ordinary skill in the art, "silicon oxide" is not a semiconductor. "Silicon oxide" is generally an insulator; whereas, a "semiconductor" is semiconductive. As such, a "silicon oxide film" cannot reasonably correspond to a "semiconductor island." Therefore, the Applicant respectfully submits that Nishitoba and Yamazaki '825, either alone or in combination, do not teach or suggest a same semiconductor island.

Since Nishitoba and Yamazaki '825 do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraph 7 rejects claims 32-37 under 35 U.S.C. 112, first paragraph, "as failing to comply with the written description requirement" (page 7, Paper No. 20091105). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. In re Marzocchi, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971). Therefore, the examiner must have a reasonable basis to challenge the adequacy of the written description and has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. In rejecting a claim, the examiner must set forth express findings of fact regarding the above analysis which support the lack of written description conclusion. See MPEP § 2163.

Claims 32-37 recite that a semiconductor island comprises a channel forming region of a first transistor and a second transistor, which is supported in the present specification, for example, by Figure 5 (reproduced and annotated below). Figure 5 shows an example of a first transistor and a second transistor sharing a same semiconductor island.




insulating layer 602 therebetween (see also paragraph [0051] of the original specification).

The Applicant respectfully submits that claims 32-37, when read in light of the specification, are adequately described and supported in the specification and that the claims and specification would reasonably convey to one skilled in the relevant art that that the inventor had possession of a manufacturing method as claimed. The Official Action fails to establish by a preponderance of evidence that such possession has not been conveyed. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 112 are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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